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1.0 Introduction

In high speed data conversion, a Track-and-Hold Amplifier (THA) is typically used within the Analog-Digital Converter (ADC), or as a separate component preceding it, to condition the signal for acquisition by the converter. The THA samples the input signal at a precise time instant and holds the value of the sample constant during the analog-to-digital conversion. This process results in signal sampling by one low jitter sampler and it reduces the ADC dynamic linearity requirements. However, the internal track-and-hold of the ADC, is not optimized for ultra wideband operation and the ADC generally has limited bandwidth and degraded high frequency linearity.

These limitations can be overcome using Hittite's HMC661LC4B ultra wideband Track-and-Hold Amplifier which is designed for use in microwave data conversion applications requiring maximum sampling bandwidth, high linearity over a wide bandwidth, and low noise. The HMC661LC4B offers 18 GHz input bandwidth and excellent broadband linearity and is used as an external master sampler at the front end of the ADC. Once extended bandwidth sampling takes place within the HMC661LC4B, the low bandwidth held output waveform can by processed by an ADC with substantially reduced bandwidth. ADC linearity limitations at high input frequencies are also mitigated because the settled THA waveform is processed with the optimal baseband linearity of the ADC. Additionally, the HMC661LC4B offers very low random sample jitter of <70 fs which minimizes jitter induced signal-to-noise (S/N) ratio degradation at high microwave signal frequencies. This jitter is significantly better than that typically obtained from currently available ADCs. The result is a radical extension in input bandwidth, substantial improvement in high frequency linearity, and improved high frequency S/N ratio for the THA-ADC assembly compared to the performance of the ADC alone.

This application note describes the performance that can be achieved when the THA is interfaced to some high speed ADCs using a typical laboratory breadboard assembly for evaluation. Example results are provided for the HMC661LC4B used as a master sampler for the National Semiconductor ADC12D1600 1.6 GS/s, 12-bit dual ADC and the Texas Instruments ADS5400 1GS/s, 12-bit ADC. Detailed guidelines on setup and interfacing of the HMC661LC4B to an Analog-to-Digital Converter may be found in Hittite's application note; General Guidelines & Procedures for using the HMC661LC4B with an Analog-to-Digital Converter.

2.0 Track-and-Hold-Analog-to-Digital Converter Breadboard Conversion Assembly Test Results

The analog-to-digital conversion assemblies consist of a breadboard type setup using the HMC661LC4B evaluation board and the evaluation board of the ADC. The performance of the ADC alone, as well as the composite THA-ADC assembly, is measured in non-interleaved mode and key performance parameters for both scenarios are then plotted and compared. For these measurements, the forward wave input RF signal level to the ADC or the HMC661LC4B is precisely leveled across frequency using an automated test system to achieve constant input amplitude. This enables measurement of the sampling transfer function and linearity at precise drive levels. The PC software provided with the ADC evaluation/reference boards is used for the ADC output data acquisition and FFT spectral analysis except in a few cases where output data time records are processed in MATLAB computation software to inspect the averaging properties of the noise floor.

Signal frequencies are chosen so that the input signal is exactly periodic over the 16 Kpoint FFT transform record for each frequency, thus avoiding spectral leakage. These frequencies fall within the bandwidth of the 5% fractional bandwidth bandpass filters present in our input signal switch matrix system that allow rapid switching of input frequency while insuring that the signals are well filtered. The frequency plans for 1.0 GS/s and 1.6 GS/s sample rate are shown in Table 1 and Table 2 respectively in the Appendix.

2.1 Hittite's HMC661LC4B / National Semiconductor ADC12D1600

Using the National Semiconductor ADC12D1600 converter, only one of the two ADCs in the dual configuration is driven by the HMC661LC4B THA. The converter is evaluated for both 1 GS/s and 1.6 GS/s sample rates. The National Semiconductor converter has a full scale input level of 800 mVp-p whereas the HMC661LC4B has a full scale capability of 1 Vp-p. Since there is a small mismatch in the full scale levels, the user has two options:

1) Directly connect the HMC661LC4B output to the converter and operate the THA at -2 dB full scale (which degrades THA S/N ratio by 2 dB but improves linearity slightly.

2) Use 2 dB of output attenuation on the THA outputs and operate both the THA and the ADC near full scale input levels.

The HMC661LC4B is a fully analog device and there is no difficulty operating at full scale or greater than full scale other than the SFDR decrease at higher input levels. The THA exhibits close to proper nonlinearity order dependence so users can calculate what spurious-free dynamic range (SFDR) impact they should expect from drive levels up to about 1.4 Vp-p. By doing this and using attenuation at the output of the THA users can improve the S/N ratio at the expense of linearity to optimize performance for their particular application. In this testing, we chose to directly connect the THA to the ADC and operate the ADC at -0.75 dBFS thus improving THA linearity slightly at the expense of THA S/N ratio. The 18 GHz THA front-end bandwidth causes the overall noise floor of the THA-ADC combination to be primarily dominated by the THA. In THA-ADC converter assembly measurements, the input level to the THA is leveled across frequency. In ADC-only measurements the input to the ADC is leveled across the frequency. This leveling produces ADC signal outputs in the range of 0 to -1 dBFS for all measurements.

A typical FFT output spectrum plot for the THA-ADC combination operating at 1.6 GS/s sample rate and 4.04 GHz input frequency is shown in Figure 1. The fundamental beat product for this scenario lands at about 759 MHz (fsig – 3 fclk). It can be seen in the plot that the SFDR is limited by a 3rd order beat product (3*fsig – 8*fclk) to approximately 57 dB at this input frequency. This SFDR goes well beyond what could be obtained from the converter by itself at this input frequency. In most of the measurements of the THA-ADC combination near full scale input we find that the SFDR is typically limited by 3rd order products.
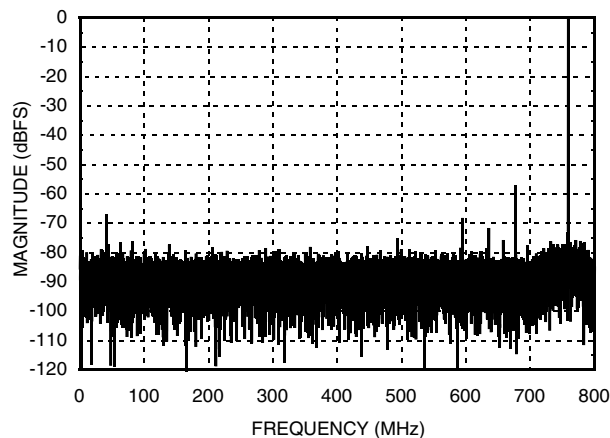

Figure 1. Typical FFT Output Spectrum for the THA-ADC Combination

Figure 2 shows the measured sampling transfer functions for both the ADC-only and the THA-ADC combination at 1.0 GS/s sample rate. The 18 GHz bandwidth HMC661LC4B radically enhances the sampling bandwidth well beyond the 2.8 GHz ADC bandwidth. This bandwidth is obtained because the HMC661LC4B takes on the burden of sampling and produces a low frequency held output waveform that is subsequently sampled by the ADC. The bandwidth of the ADC internal THA then has little impact on the overall bandwidth. The small ripples in the frequency response are caused by small levels of reflections on the evaluation board and cable interconnects between the THA and the ADC chips. Even with these perturbations, which would be reduced in an integrated board implementation, the response is flat to approximately ±0.5 dB across 12 GHz. The sampling transfer function is not particularly dependent on the sampling frequency as long as this sample rate falls within the capability of the ADC and the THA. Similar results are obtained for operation at 1 GS/s sampling rate. (Please refer to the HMC661LC4B product data sheet for sampling transfer function of the THA which is down by -3 dB at 18 GHz.)
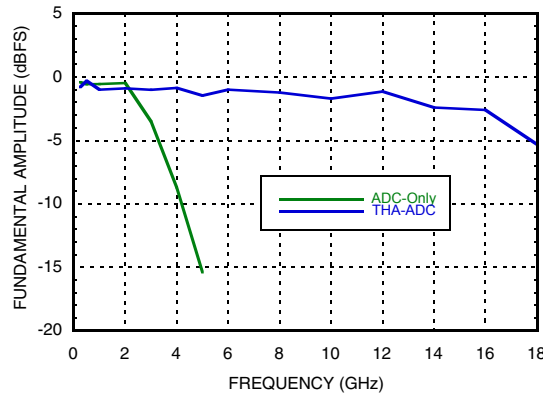
Figure 2. Measured Sampling Transfer Functions for both ADC-Only & THA-ADC
(National ADC12D1600 @ 1 GS/s)

The time domain S/N ratio (obtained by integrating the noise spectral density over the Nyquist interval) and SFDR for the ADC-only and the THA-ADC combination at 1 GS/s and approximately -0.75 dBFS input level are shown in Figure 3. Comparison of the SFDR curves shows that the HMC661LC4B not only enhances the SFDR beyond the bandwidth of the ADC but also enhances it for frequencies within the 2.8 GHz ADC bandwidth by up to 11 dB. This enhancement occurs because the HMC661LC4B provides high linearity sampling of the high frequency signals and the constant amplitude held output waveform presented to the ADC mitigates the slew rate dependent distortion created within the ADC's internal THA. The Effective-Number-of-Bits (ENOB) and Signal-to-Noise-And-Distortion (SINAD) which represent the total effects of random noise and nonlinearity products are improved for frequencies beyond about 3 GHz.
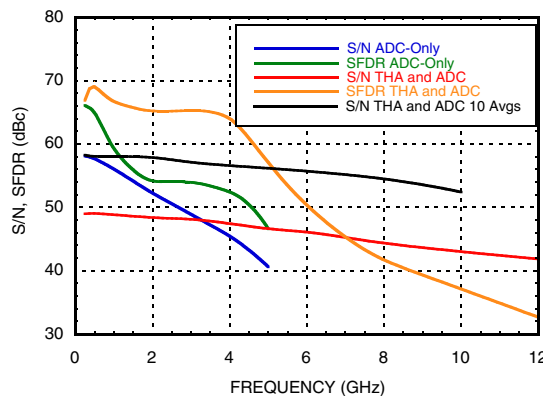

Figure 3. Time Domain Signal-to-Noise & SFDR for the ADC-only & THA-ADC
(National ADC12D1600 @ 1 GS/s)

The expansion of the front end bandwidth to 18 GHz creates an unavoidable increase in noise floor for the THA-ADC combination at low frequencies where the ADC thermal noise tends to dominate, but the ADC noise degradation created at higher input frequencies by the digitization noise is actually mitigated by the THA signal conditioning. This can be seen in the improved S/N ratio for the THA–ADC combination above approximately 3 GHz signal frequency. The HMC661LC4B THA mostly preserves the inherent equivalent input noise spectral density of the ADC. The difference in noise levels at baseband (250 MHz) is about 8.5 dB compared to the 8.1 dB ratio of the bandwidth expansion (10 log (18/2.8)=8.1 dB). Hence, the total noise of the THA-ADC combination is nearly the same as would be obtained if the ADC had its input bandwidth increased to 18 GHz (with the same noise equivalent input spectral density). The decreasing S/N ratio with increasing frequency of the THA-ADC

combination is due to random sample jitter resulting from about 70 fs of HMC661LC4B THA jitter and about 54 fs of clock generator noise-induced jitter (total sample jitter of approximately 88 fs). The generator noise induced jitter is easily identified by the fact that the bandwidth of the sidebands it produces on the converted signal exactly matches the bandwidth of the filter on the clock signal. This clock generator noise effect is shown in detail in the FFT spectrum plot of Figure 4 for the case of 1.6 GS/s sample rate and approximately 10.1 GHz input signal frequency. Here, the band limited jitter sideband noise on the fundamental due to the signal generator broadband noise that escapes through the 50 MHz bandwidth of the bandpass clock filter can easily be observed. This level of jitter is set by the output S/N ratio of the signal generator itself. In an optimized system, the clock filter bandwidth (5% fractional bandwidth = 50 MHz in this test setup) would be reduced to a much narrower bandwidth to reduce the impact of the generator noise, thus approaching an overall jitter level dominated by the 70 fs THA jitter.
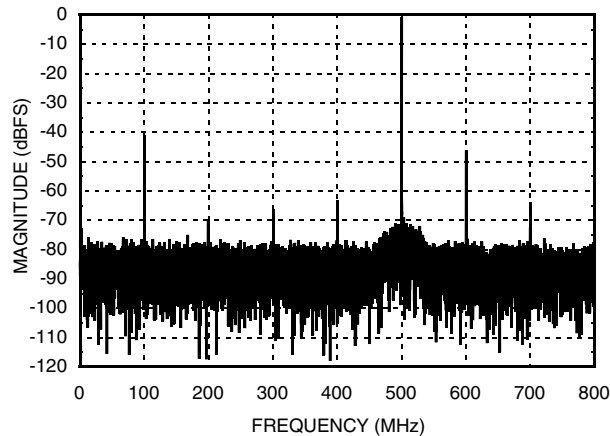

*Figure 4. THA-ADC FFT Output Spectrum Showing Phase Noise Sidebands
on the Fundamental Beat Product Induced by Clock Generator Noise.*

Users performing post-conversion signal processing are usually concerned about the noise floor reduction that can be obtained through averaging processes, either arising from direct averaging of multiple data records or the processing gain resulting from spread spectrum processing. We took a 32K point data record at each frequency and broke it up into as many as 16 independent, but signal-phase-coherent 2K point records to test the noise averaging properties of the THA-ADC combination noise floor, as well as the ADC-only noise floor. Figure 3 shows that 10 averages of the complex FFT data reduces the noise floor by about 9 to 10 dB (while holding the signal constant). This demonstrates that the THA noise floor is truly random and functions well under averaging since it is a linear analog device with white noise floor. The lower frequencies tend to show averaging improvement of 9 dB. This shortfall, relative to the ideal 10 dB expected from 10 averages, is caused by the ADC noise floor contribution which does not completely average as a random signal. The ADC contribution to the averaged noise floor tends to limit at a S/N ratio of approximately 63 dBFS regardless of the number of averages.
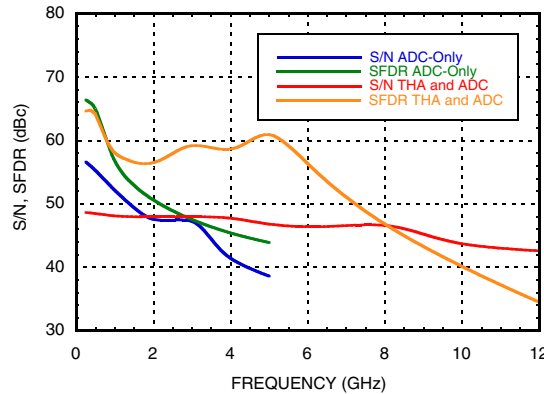
*Figure 5. Signal-to-Noise & SFDR vs. Signal Frequency for the ADC-only & THA-ADC
(National ADC12D1600 @ 1.6 GS/s)*

Similar performance trends for S/N ratio and SFDR are obtained at a clock rate of 1.6 GS/s as shown in Figure 5. The intrinsic linearity of the ADC is reduced at this sample rate which is at the upper limit of capability for this converter. However, even in this case, the THA provides a substantial improvement in SFDR beyond 1 GHz signal frequency and an ENOB improvement beyond about 2 GHz signal frequency. Additional improvement of the ENOB at both clock frequencies could be obtained by driving the THA at 1 Vp-p full scale and using a small amount of attenuation between the THA and the ADC to match the full scale levels for the two devices as described earlier.

2.2   Hittite's HMC661LC4B / Texas Instruments ADS5400

The Texas Instruments ADS5400 1 GS/s, 12-bit converter has a full scale input range which is adjustable within the range of 1.5 Vp-p to 2 Vp-p. The noise level does not appear to significantly change with full scale input setting so operation of the converter at 1.5 Vp-p full scale results in 2.5 dB of S/N ratio loss relative to what is obtained for the 2 Vp-p input level. Since the full scale input level of the THA is 1 Vp-p, the optimal S/N can be obtained by adding an amplifier with about 5 to 6 dB of gain such that the THA full scale level drives the ADC at its 2 Vp-p full scale level. The amplifier should support the input bandwidth of the ADC in order to maintain the ADC sample rate capability since the ADC acquisition time is impacted by input bandwidth.

The ADC was driven with the un-amplified output of the HMC661LC4B, fully accepting the S/N ratio loss associated with driving the converter under its full scale value. The full scale value of the converter was set to 1.5 Vp-p. When the HMC661LC4B is driven at 1 Vp-p input level, the resultant ADC drive level under these conditions is about -5.5 dBFS. This is the result of -3.5 dB of full scale level mismatch relative to the 1.5 Vp-p full scale level (20* log(1/1.5) = -3.5 dB), plus about -1 dB of baseband gain in the HMC661LC4B and about -1 dB of microstrip loss in the ADC evaluation board. In order to get a fair comparison between the ADC-only and THA-ADC measurements for this configuration, we evaluated the ADC-only scenario at a maximum input level of -2 dBFS which is exactly 3.5 dB (the full scale mismatch ratio in dB) above the -5.5 dBFS level achieved when driving the THA-ADC combination. This gives a S/N ratio difference between the ADC-only and THA-ADC configurations that is an upper bound on the difference that would be obtained if a "makeup" amplifier gain appropriate for the ADC's 1.5 Vp-p full scale setting were used.

Figure 6 shows the measured sampling transfer functions for both the ADC-only and the THA-ADC combination at 1 GS/s sample rate. As with the National Semiconductor converter, the HMC661LC4B radically enhances the sampling bandwidth well beyond the intrinsic ADC bandwidth.
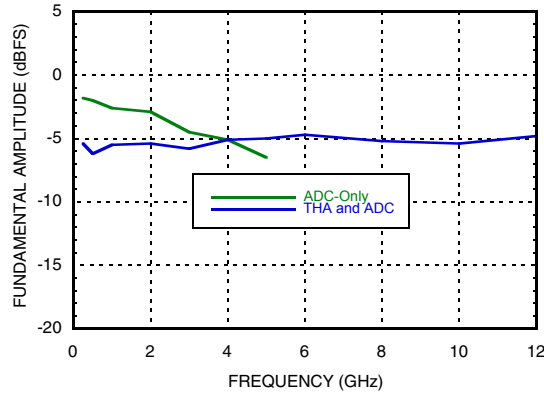
Figure 6. Sampling Transfer Functions for ADC-only & THA-ADC (TI ADS5400 @ 1 GS/s)

Figure 7 shows the time domain S/N ratio and SFDR for the ADC alone and the THA - ADC combination at 1 GS/s when the THA is driven at full scale input (1 Vp-p) without a "makeup" gain interface amplifier as previously discussed. The HMC661LC4B provides substantial SFDR improvement beyond 2 GHz and ENOB improvement beyond 3 GHz. As with the National Semiconductor converter, the expanded bandwidth introduces additional unavoidable noise to the combined assembly but the effective input noise spectral density of the ADC is well maintained by the THA since the change in S/N ratio introduced by the THA is less than the ratio of the bandwidth expansion. The inclusion of an appropriate "makeup" gain amplifier that matches the full scale level of the THA to the ADC would provide another 4 dB or so of S/N ratio improvement on the performance shown in Figure 7.
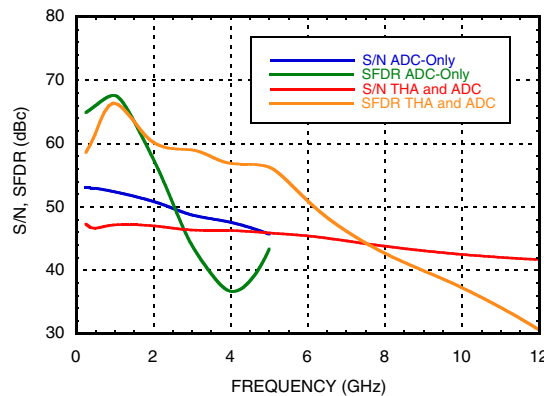

*Figure 7. Signal-to-Noise & SFDR vs. Signal Frequency for the ADC-only & THA–ADC
(TI ADS5400 @ 1GS/s)*

3.0 Summary

This application note discusses the use of Hittite's HMC661LC4B Ultra Wideband Track-and-Hold Amplifier (THA) for bandwidth and linearity enhancement in high speed Analog-to-Digital Converters. Measurements of the performance obtained when the HMC661LC4B is used as a master sampler for some current state-of-the-art high speed converters are presented. The results demonstrate that the HMC661LC4B can radically extend the bandwidth of existing high speed ADCs while also providing enhanced high frequency linearity and noise performance relative to that obtained with the converter alone. For the tested National Semiconductor converter at 1 GS/s, the HMC661LC4B provides Effective Number of Bits (ENOB) improvement beyond 3 GHz. At 1.6 GS/s the THA provides an ENOB improvement beyond about 2 GHz. Similar performance enhancement is also measured for the Texas Instruments ADS5400 1 GS/s ADC. This performance enhancement should be useful in a variety of applications requiring A/D conversion at wide bandwidths or high center frequencies that are beyond the reach of the existing high speed converters.

Detailed guidelines on setup and interfacing of the HMC661LC4B to an ADC may be found in Hittite's application note General *Guidelines & Procedures for using the HMC661LC4B with an Analog-to-Digital Converter*.

4.0 Appendix

Table 1. 1.0 GS/s Frequency Plan for THA

ADC evaluation at 1 GS/s that eliminates spectral leakage in the 16k point FFT by satisfying the criteria n/fsig=m/fclk, m=2^14

n	fsig (MHz)
4139	252.6245117
8273	504.9438477
16547	1009.94873
33091	2019.714355
49639	3029.724121
66191	4039.978027
82729	5049.377441
99289	6060.119629
132383	8080.01709
165479	10100.03662
198571	12119.81201

Table 2. 1.6 GS/s Frequency Plan for THA

ADC evaluation at 1.6 GS/s that eliminates spectral leakage in the 16k point FFT by satisfying the criteria n/fsig=m/fclk, m=2^14

n	fsig (MHz)
2591	253.0273438
5171	504.9804688
10343	1010.058594
20681	2019.628906
31033	3030.566406
41381	4041.113281
51713	5050.097656
62057	6060.253906
82757	8081.738281
103423	10099.90234
124121	12121.19141